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FACSIMILE COVER LETTER

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FROM: James J. Murphy

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Applicant: Axel Thomsen

Serial No.   09/695,706

Filing Date: October 25, 2000

Title: **TECHNIQUES FOR SIGNAL MEASUREMENT USING A
CONDITIONALLY STABLE AMPLIFIER**

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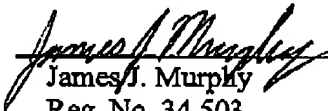
Group Art Unit: 2816

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TRANSMITTAL OF FORMAL DRAWINGS

Transmitted herewith are twenty-three (23) sheets of formal drawings (one of
which is a replacement sheet) to be substituted for the drawings filed November 24, 2004
in connection with the above-identified application for patent.

Respectfully submitted,
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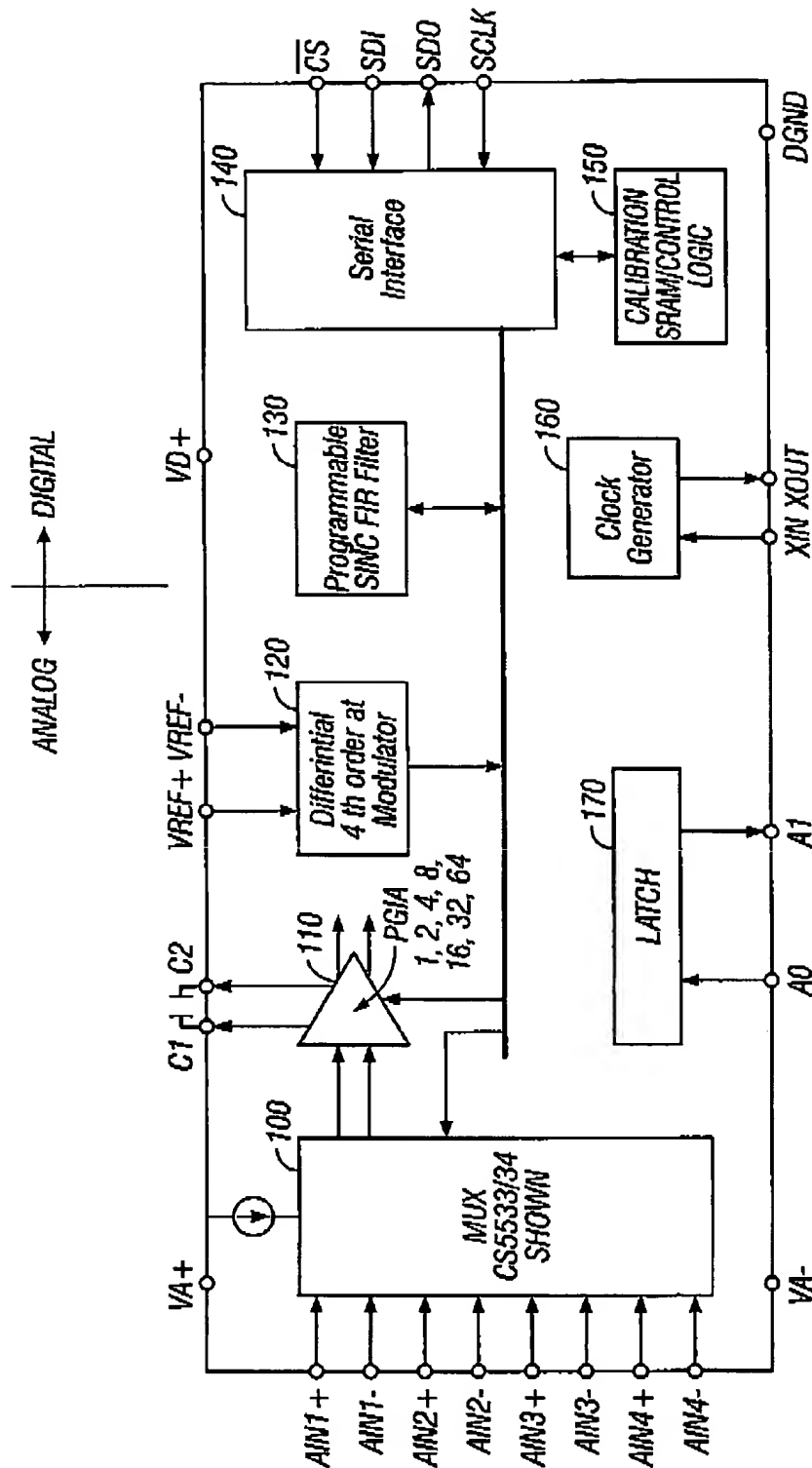
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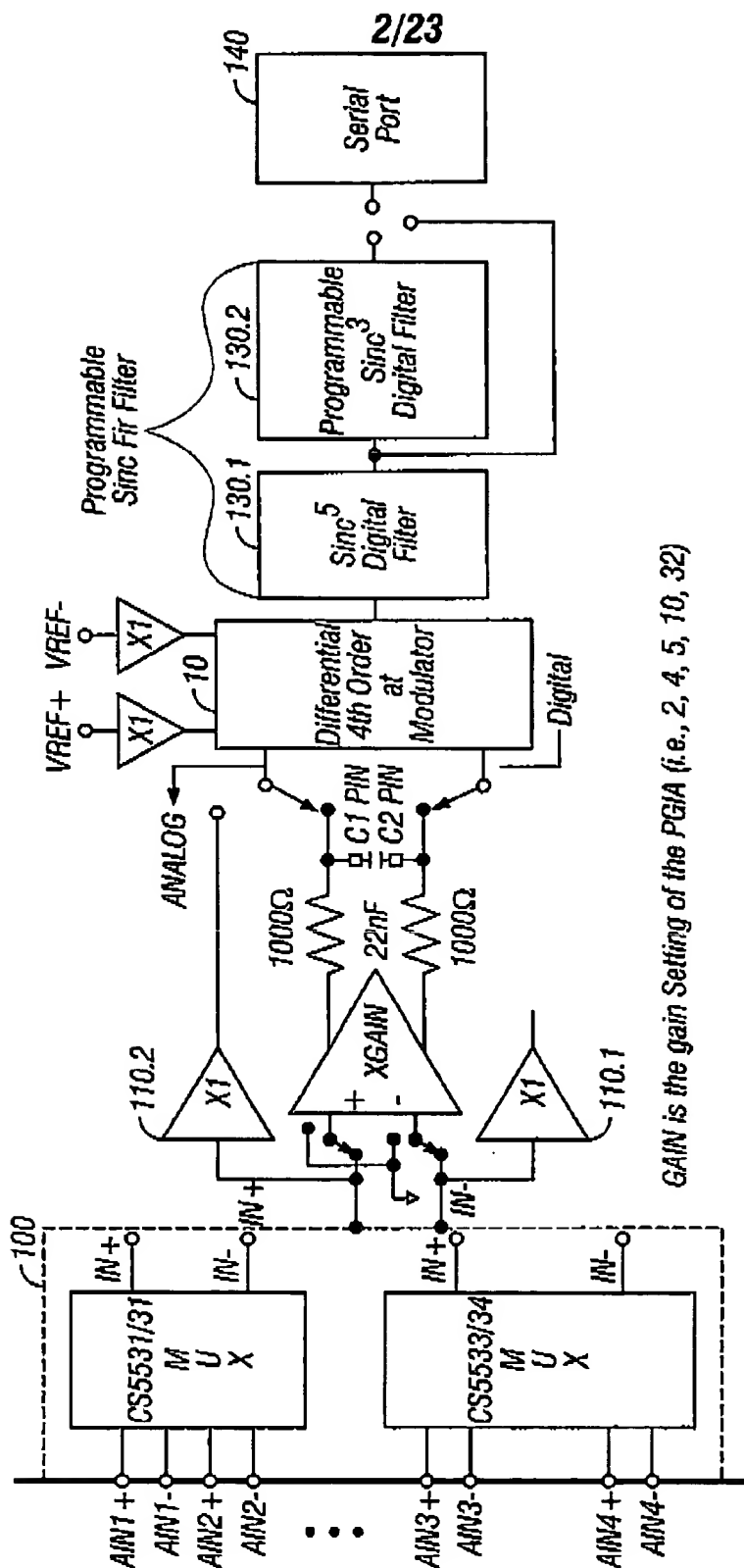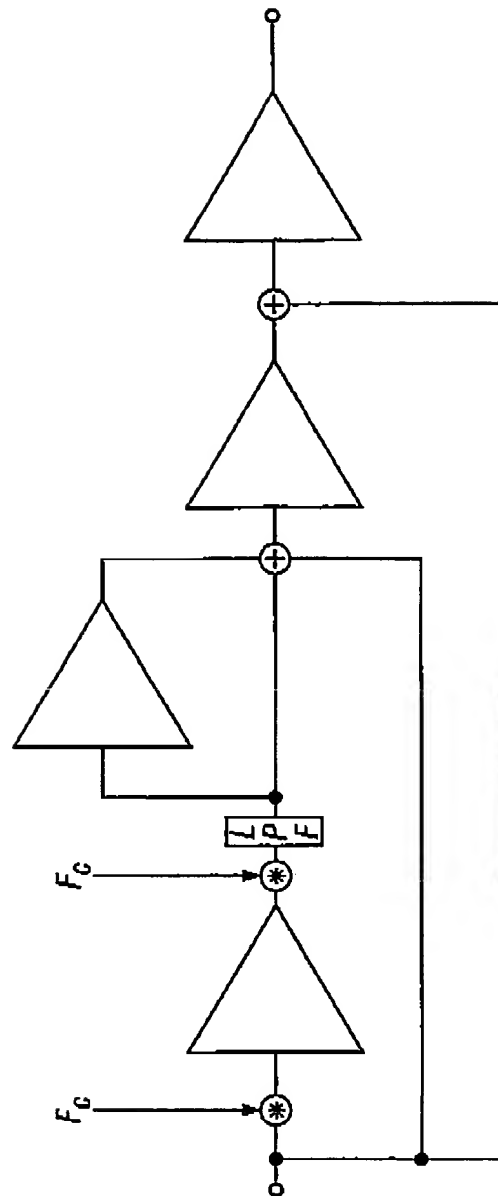
REPLACEMENT
SHEET

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FIG. 1.1

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Serial
Port
140

Programmable
Sinc Fir Filter

Programmable
Sinc³
Digital Filter
130.2

Sinc⁵
Digital
Filter
130.1

VREF+ VREF-

X1   X1
10

Differential
4th Order
at
Modulator

Digital

ANALOG

C1 PIN
C2 PIN

1000Ω   22nF   1000Ω

XGAIN

+ -

110.2 X1   X1 110.1

IN+   IN-

IN+   IN-

100

CS5531/31
M
U
X

IN+   IN-

CS5533/34
M
U
X

IN+   IN-

AIN1+ AIN1- AIN2+ AIN2-   • • •   AIN3+ AIN3-   AIN4+ AIN4-

GAIN is the gain Setting of the PGIA (i.e., 2, 4, 5, 10, 32)

FIG. 1.2

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FIG. 1.3

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FIG. 1.4

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DIGITAL BLOCK DIAGRAM

FIG. 1.5

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FIG. 1.6

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FIG. 2.0

FIG. 2.1

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V_{IN} = CONSTANT

$V_{OUT} > V_x$

Voltage V_{out}

V_{IN}

TIME

Beginning of Phase 1
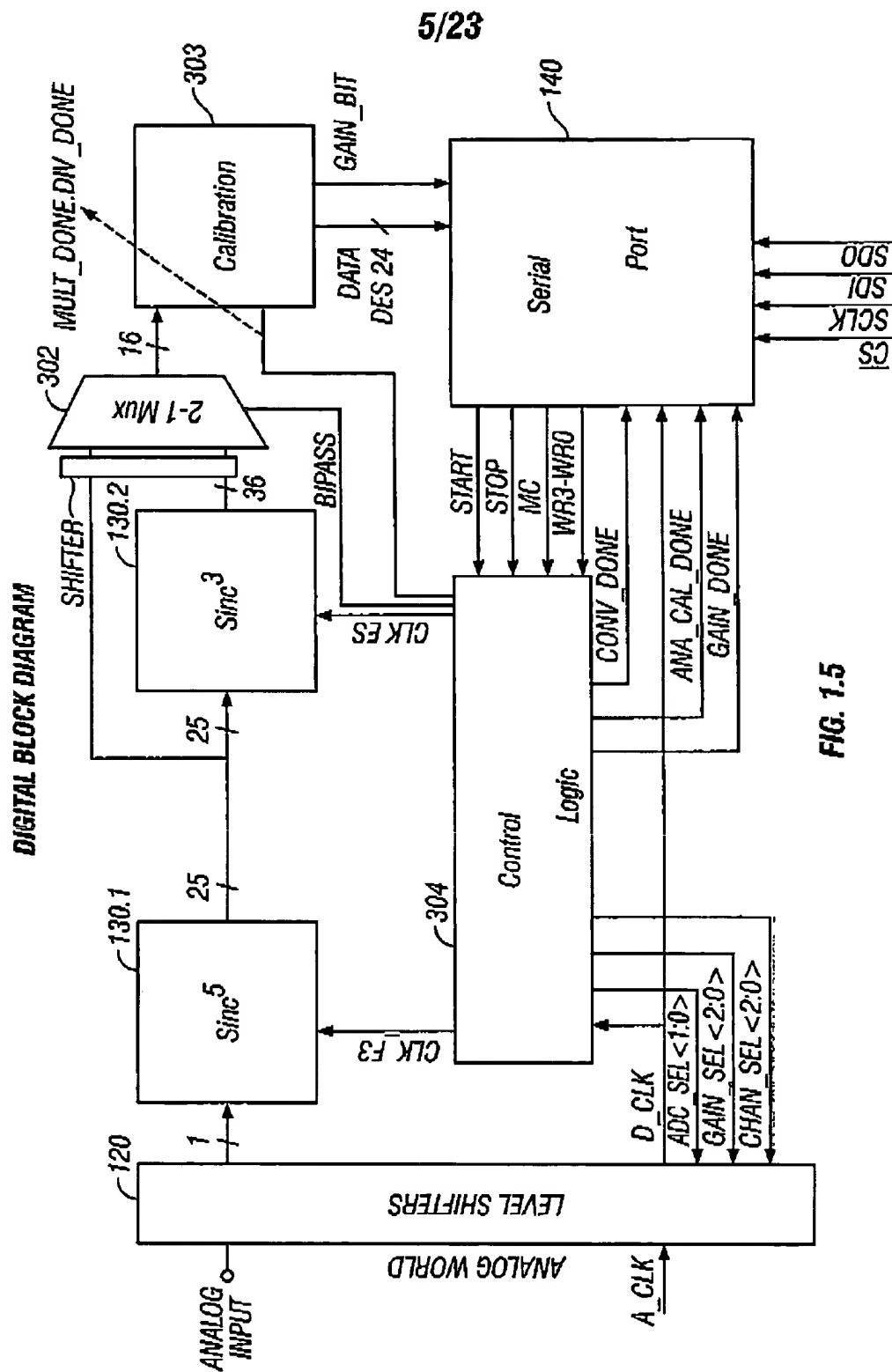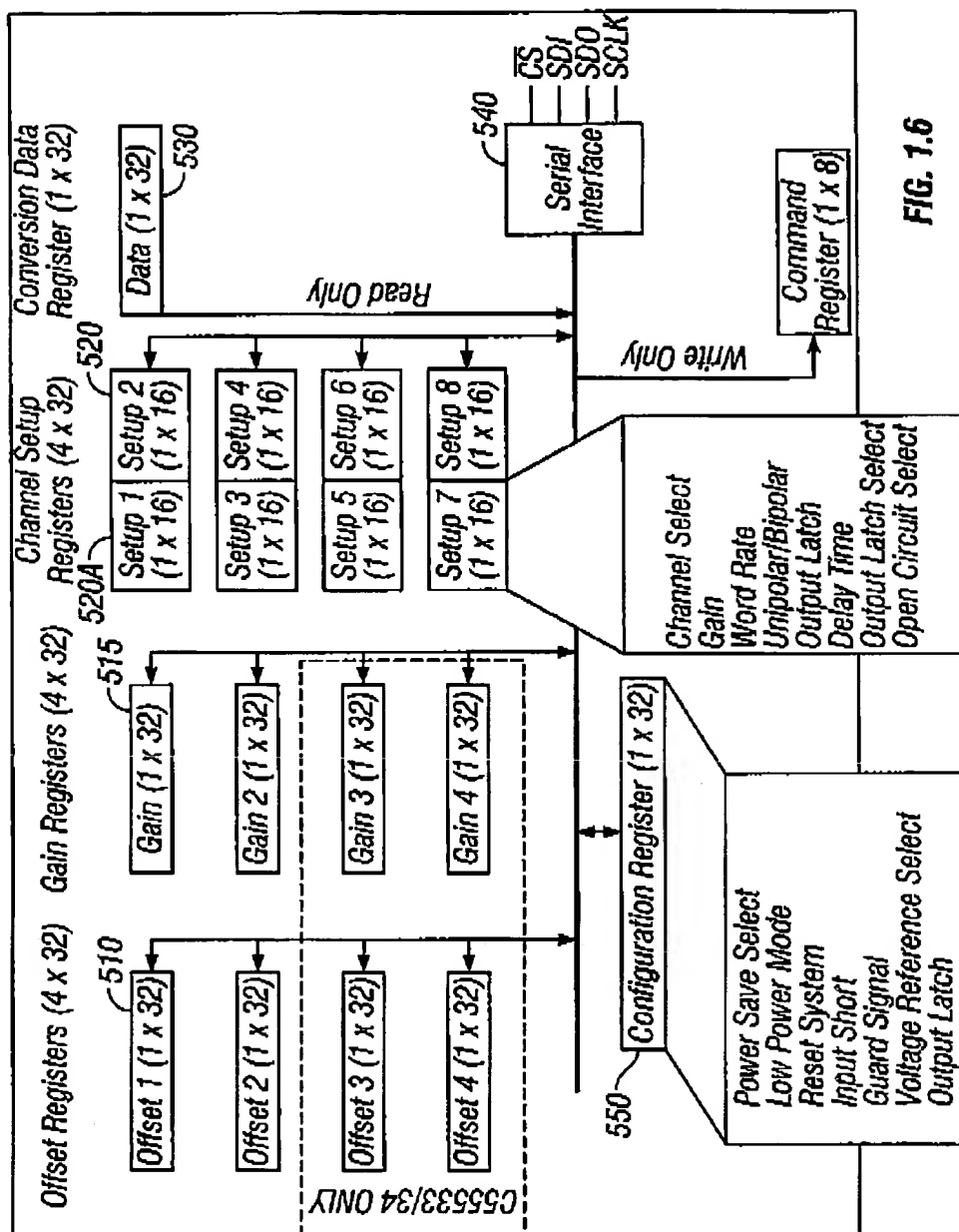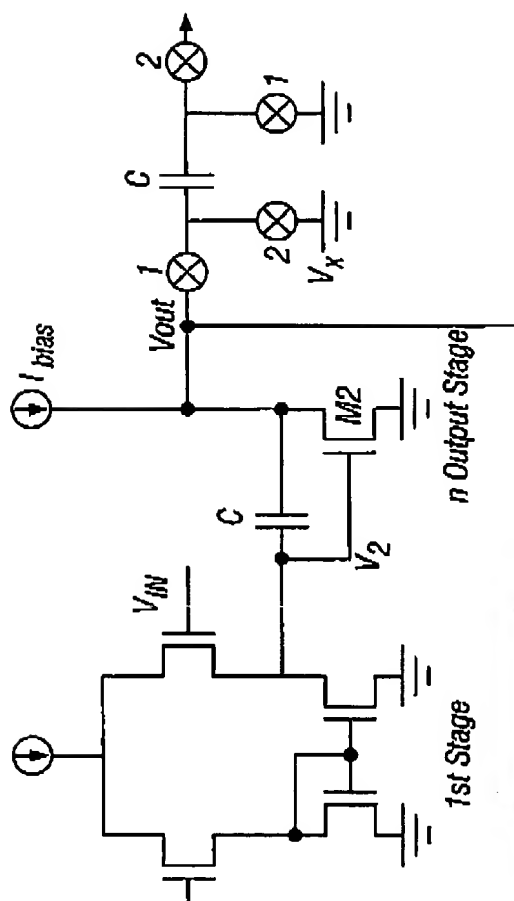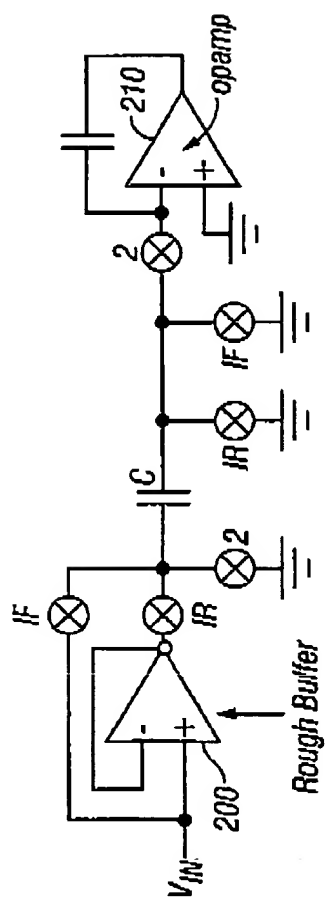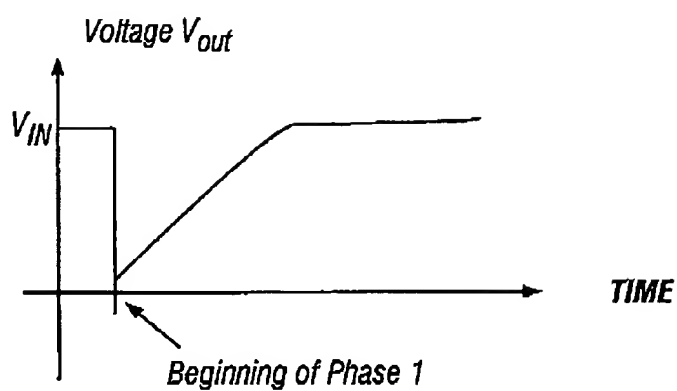
FIG. 2.2

V_{IN} = CONSTANT

$V_{OUT} < V_x$

TIME
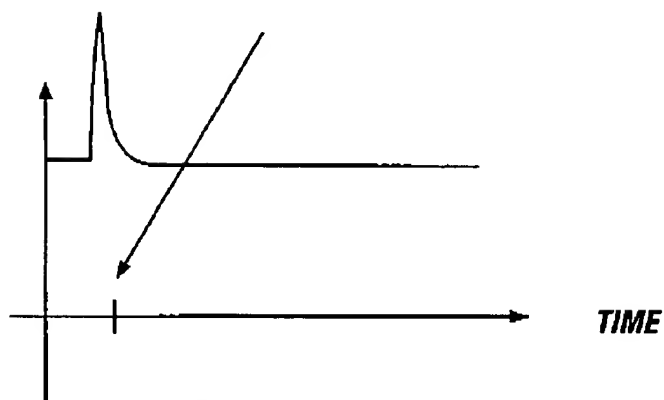
FIG. 2.3

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FIG. 2.4

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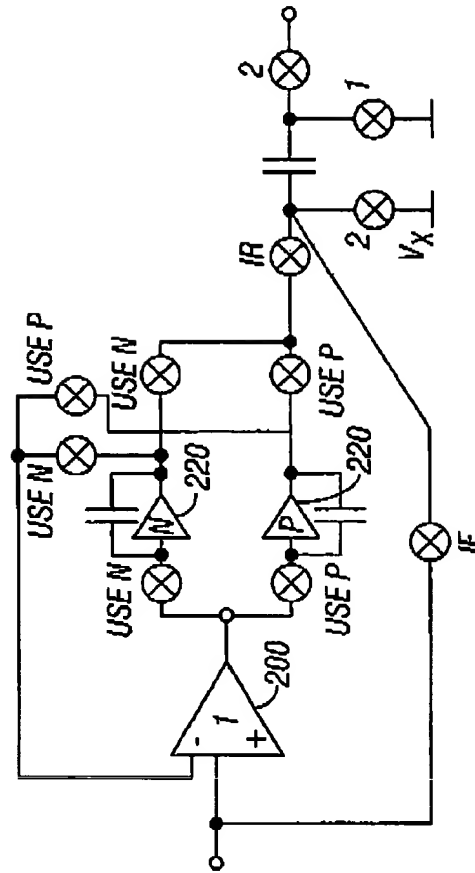
FIG. 2.5
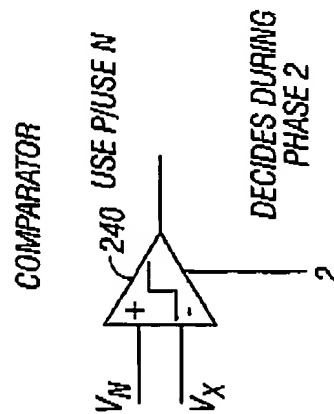
11/23
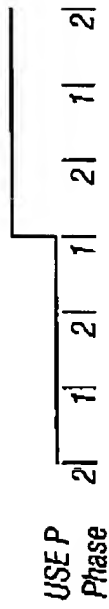
Vin

Vx

FIG. 2.6

USE P
Phase

2| 1| 2| 1| 2| 1| 2|

FIG. 2.7

Vout

FIG. 2.8

MULTIPLIER ARCHITECTURE
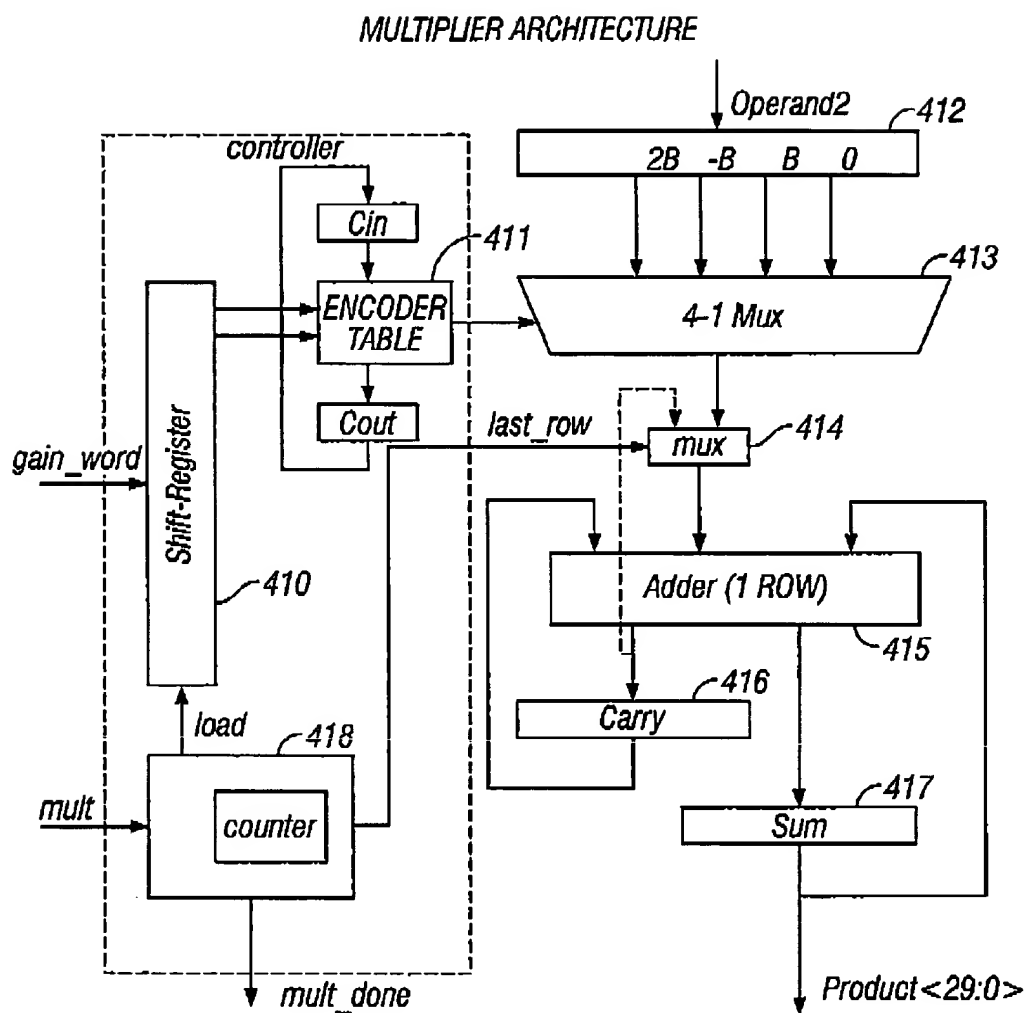
FIG. 3.1

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A_{i+1}	A_1	Operation
0	0	$R_i = R_{i-1} / 4$
0	1	$R_i = (R_{i-1} + B) / 4$
1	0	$R_i = (R_{i-1} + 2B) / 4$
1	1	$R_i = (R_{i-2} + 3B) / 4$

FIG. 3.2
(Prior Art)

Cin	A_{i+1}	A_i	Operation	Cout
0	0	0	$R_i = R_{i-1} / 4$	0
0	0	1	$R_i = (R_{i-1} + B) / 4$	0
0	1	0	$R_i = (R_{i-1} + 2B) / 4$	0
0	1	1	$R_i = (R_{i-2} - 3B) / 4$	1
1	0	0	$R_i = (R_{i-1} + B) / 4$	0
1	0	1	$R_i = (R_{i-1} + 2B) / 4$	0
1	1	0	$R_i = (R_{i-1} - B) / 4$	0
1	1	1	$R_i = (R_{i-1}) / 4$	1

FIG. 3.3
(Prior Art)

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Example 1

$A=2, B=3$ $B=0101$
$A=110010$

$$\rightarrow 2B$$
$$\rightarrow 0$$
$$\rightarrow 0$$

$$\begin{array}{r} 1 \\ 111010 \\ 110000 \\ \underline{110000} \\ 0000001010 \end{array}$$

FIG. 3.4

Example 2

$A=-2, B=1$ $B=0101$
$A=111110$

$$\rightarrow 2B$$
$$\rightarrow -B+1$$
$$\rightarrow B+1$$

$$\begin{array}{r} 1 \\ 111010 \\ 101011 \\ \underline{110000} \\ 1111110110 \end{array}$$
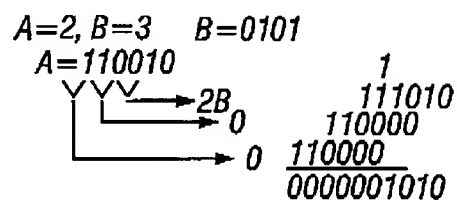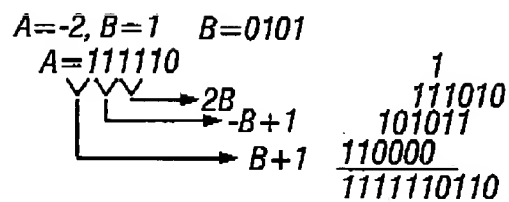
FIG. 3.5

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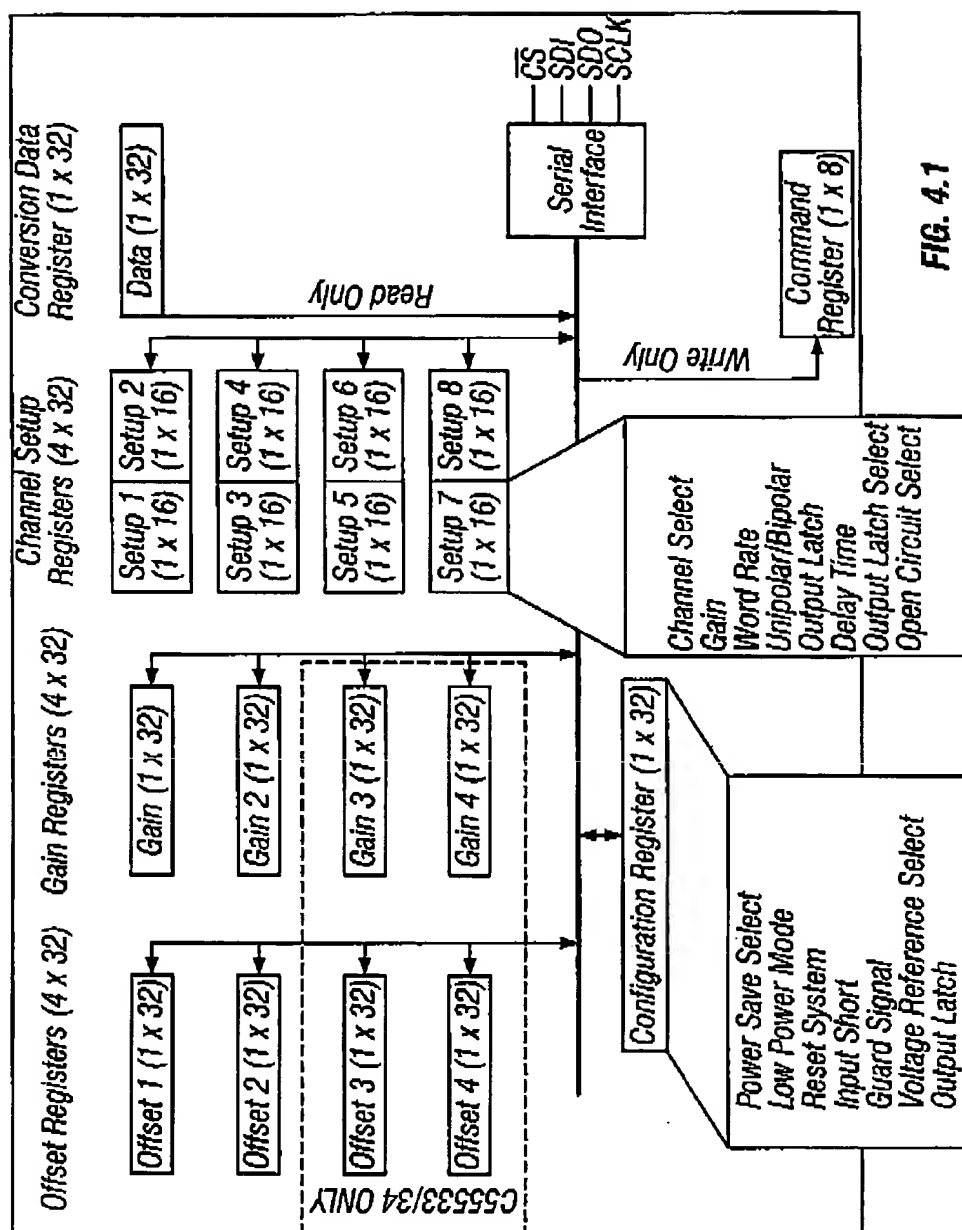
FIG. 4.1

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D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/W	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	COMMAND Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array registers. The particular registers accessed are determined by the RS bits. The register are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0)	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/Write, R/W	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

FIG. 4.2

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D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

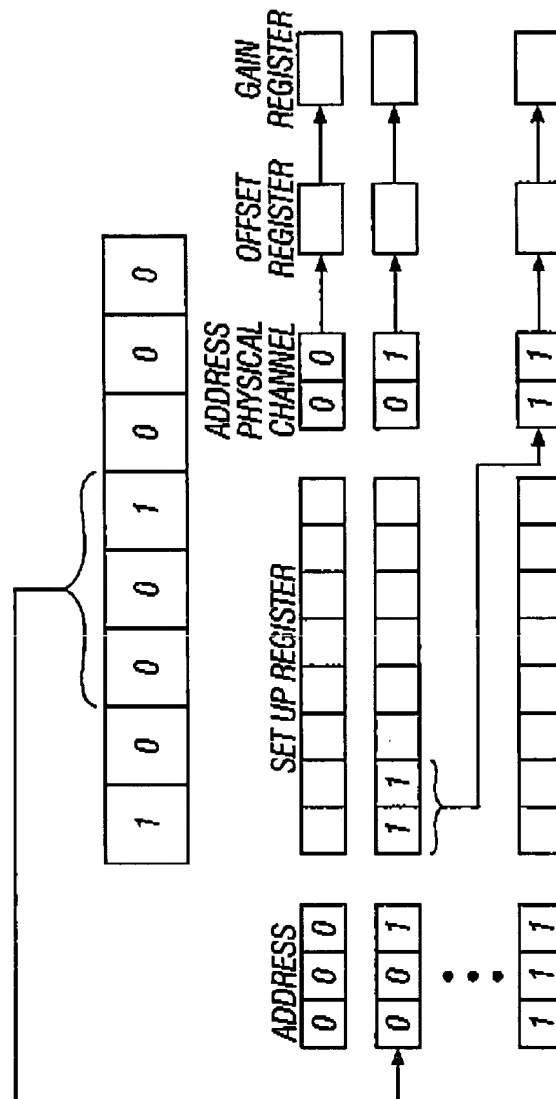| BIT	NAME	VALUE	FUNCTION
D7	COMMAND Bit, C	0 1	These commands are invalid if this bit is logic 0. Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0 1	Perform fully settled single conversions. Perform conversions continuously.
D5-D3	Channel Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are preformed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000 001 010 011 100 101 110 111	Normal Conversion Self-Offset Calibration Self-Gain Calibration Reserved Reserved System-Offset Calibration System-Gain Calibration Reserved

FIG. 4.3

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FIG. 4.4

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FIG. 4.5

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FIG. 4.6

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INTRODUCE A VALUE OF INTENTIONAL OFFSET INSIDE OF CHOPPER STABILIZED AMPLIFIER GREATER THAN THE EXPECTED VARIATION IN AMPLIFIER INPUT OFFSET

IS OUTPUT OFFSET WITHIN THE RANGE OF EXPECTED OUTPUT OFFSET IF CHOPPER AMPLIFIER IS WORKING PROPERLY?

YES

NO
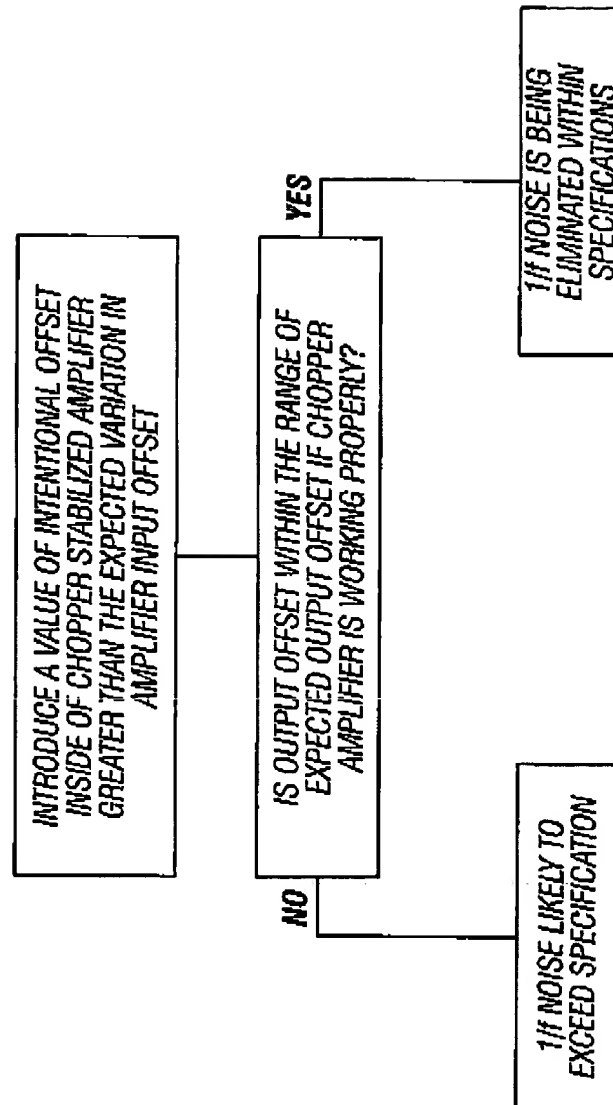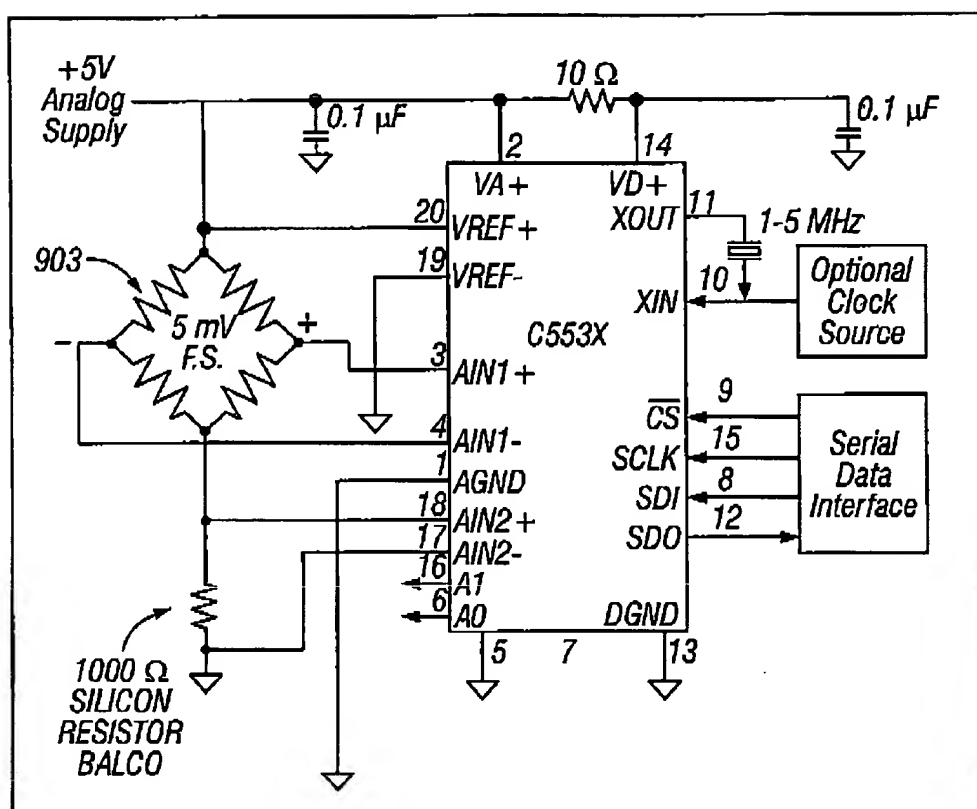
1/f NOISE IS BEING ELIMINATED WITHIN SPECIFICATIONS

1/f NOISE LIKELY TO EXCEED SPECIFICATION

FIG. 5.1

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FIG. 6.1

FIG. 6.2